

Exploring the Perceived Limits of Gallium-based Focused Ion Beam (FIB) Chip Circuit Editing

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Despite significant advances in modeling and extensive use of automated layout and checking algorithms, simple interconnect wiring mistakes and logic errors continue to happen in integrated circuit design. A single error in an advanced processor can result in several month's delay, while waiting for a new mask set and wafer Fab run to produce testable product. Last year at this conference we introduced many attendees to the concept of Focused Ion Beam (FIB) chip circuitry modification. Beam induced etch and deposition processes can be used to remove, add or modify internal interconnect wiring, or even whole transistors. As a result, FIB based circuit editing to create working prototype modules has become an important part of the time-to-market strategy for many chip makers and foundry customers.

But what are the limits of this technique? And specific to this work, what are the limitations of the current breed of gallium based FIB tools? How fine can they slice in a real-world edit operation? Where will the gallium go, and how much damage to transistor operation can we expect to see when working with a charged particle beam of metal ions?

A big factor in editing is the characteristics of the tool's primary ion beam; the 'scalpel' in this form of microsurgery. The ideal scalpel would be infinitely sharp, provide sufficient secondary electrons for great imaging and good precursor gas activation, produce surface sputtering or implantation only where or when you wanted it, and be totally non-contaminating.

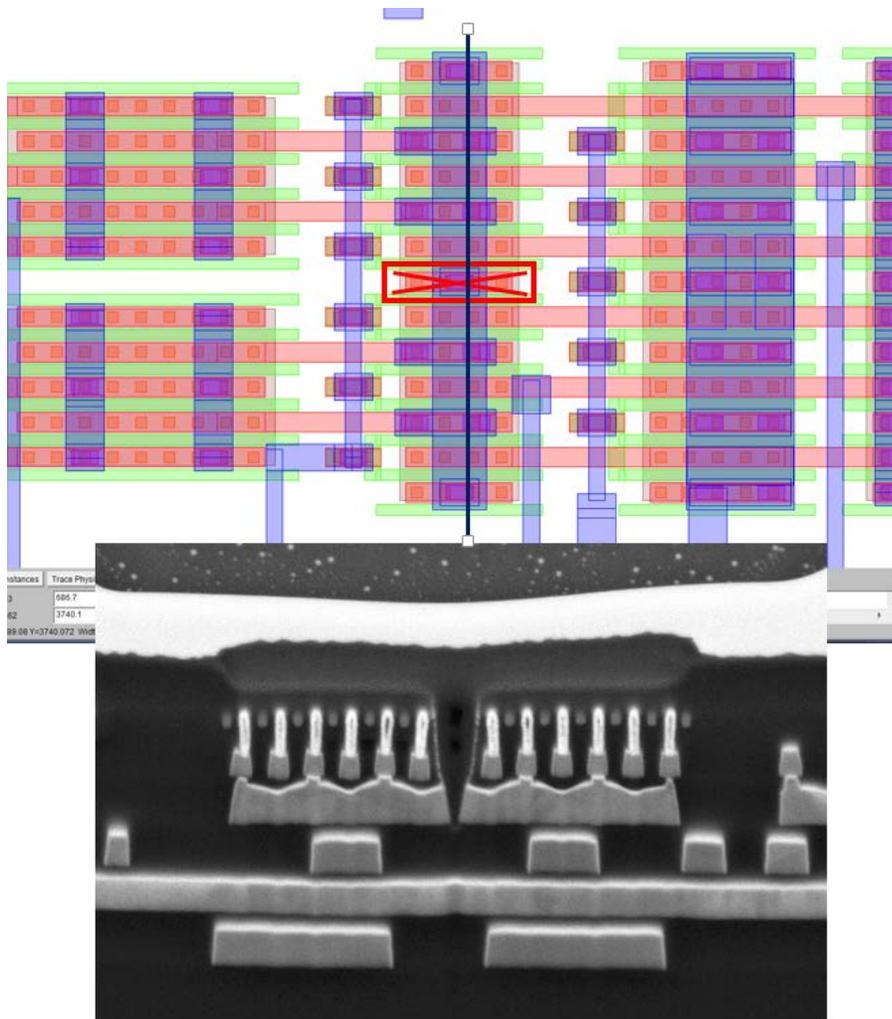
The most highly developed FIB Chip Edit platforms use Gallium as the primary ion beam source. It was a good choice in years past, but on advanced circuit nodes a number of the characteristics of this ion are becoming a limiting factor. An edit operation in close proximity to an active transistor structure is particularly risky when you can't accurately control the beam tail placement, implantation or scatter of a primary ion that is also a metal and p-type dopant.

A year ago our lab was asked to slice a 32nm technology multi-finger transistor into two halves. It became necessary when two parallel data paths in close proximity were accidentally merged one stage prior to an intended logic combination point. A pair of 6 finger inverter/driver transistors became a single 12 finger structure, intermixing the two signals and scrambling the outputs. Would it be possible to come in thru the underside and slice the structure into equal halves and restore functionality? Deleting a whole transistor or changing its placement within a circuit is commonplace. Splitting one was something we'd never done before, and at first didn't seem possible. We'd invariably introduce a dopant level that would shift transistor parameters, or enough of a metallic path to cause it to leak excessively – either to ground or the two halves to each other.

Working with an inert, non-contaminating ion source like the He⁺ – Ne⁺ FIB seemed like the best option, but we couldn't get on a system within the time required. Our only choice was to perfect a cut and

cleanup strategy for Ga⁺. The key was exact targeting to slice thru the accidentally inserted diffusion plus the via-connected M1 strip above, and the M2 conjoining bridge. Finally it would require some post processing to minimize the Ga remaining in the immediate vicinity and adjacent gate regions that were inadvertently disturbed.

The end result was a loss of two fingers at the cut site. The merged 12 finger device became two fully operational 5 finger transistors. But despite the modest loss in drive current, total functionality of the two circuits was maintained within the specified timing window, and chip-level testing was enabled.



Cross-section of cut on a practice part.