IBM

Precision, double XTEM sample preparation of site specific Si nanowires

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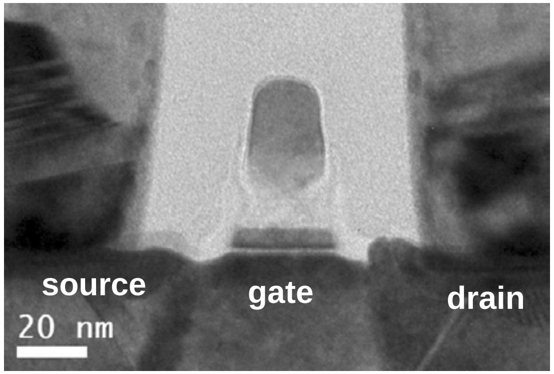
Outline

- **Background:**
  - Planar device scaling limitations
  - Si nanowires (NW) fabrication
- **1st XTEM section: along nanowire (NW) direction**
  - ex-situ lift-out on C membrane
  - measure gate length
- **2nd XTEM section (from 1st XTEM section sample): perpendicular to NW direction**
  - in-situ lift-out on Cu five-finger grid
  - measure nanowire diameter and shape
- **Conclusions**

CMOS Device Scaling Limitations

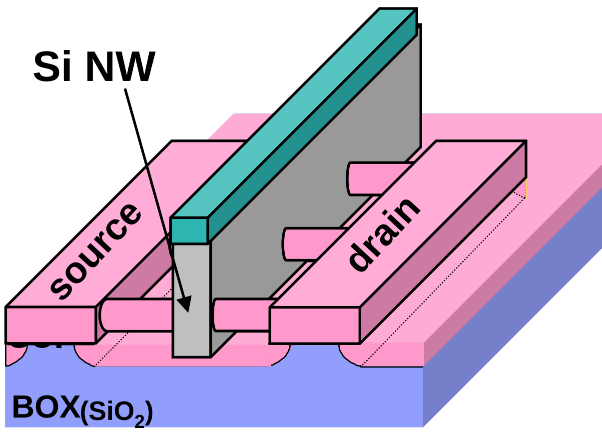
- **planar CMOS device scaling has followed Moore's Law:**
  - double in the # of transistors per chip every 2 years
- **continued scaling will hit performance limits:**
  - degraded short channel effects
  - high gate leakage due to thinning of the gate dielectric
  - reduced channel mobility due to increased doping in the channel
  - increased source/drain resistance
- **develop new materials sets**
  - high k gate dielectric (replacing SiO_2)
  - metals replacing poly-Si as gate electrode
  - high mobility channels: strained Si, SiGe, Ge
- **develop novel device structures**
  - multi-gated devices (instead of planar, single gated devices)
    - reduces short channel effect
  - **Si nanowire device has Gate All Around (GAA) structure:**
    - **best gate for electrostatic control of the channel potential**

planar CMOS device



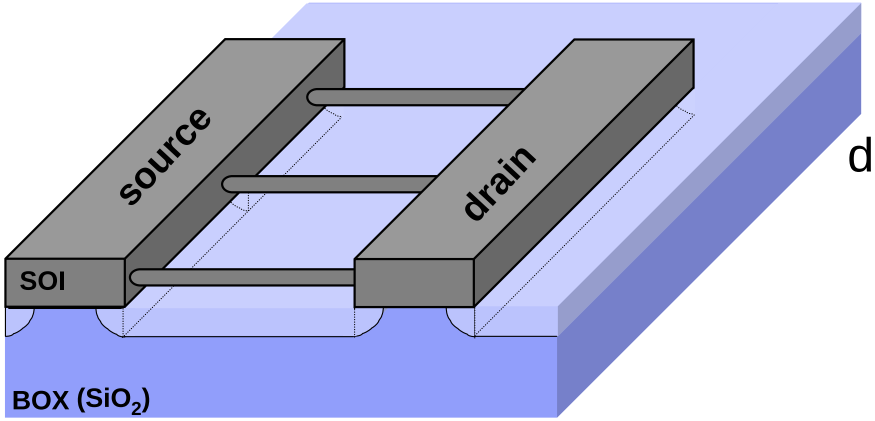
from Y. Zhu, P. Raman, A. Kumar

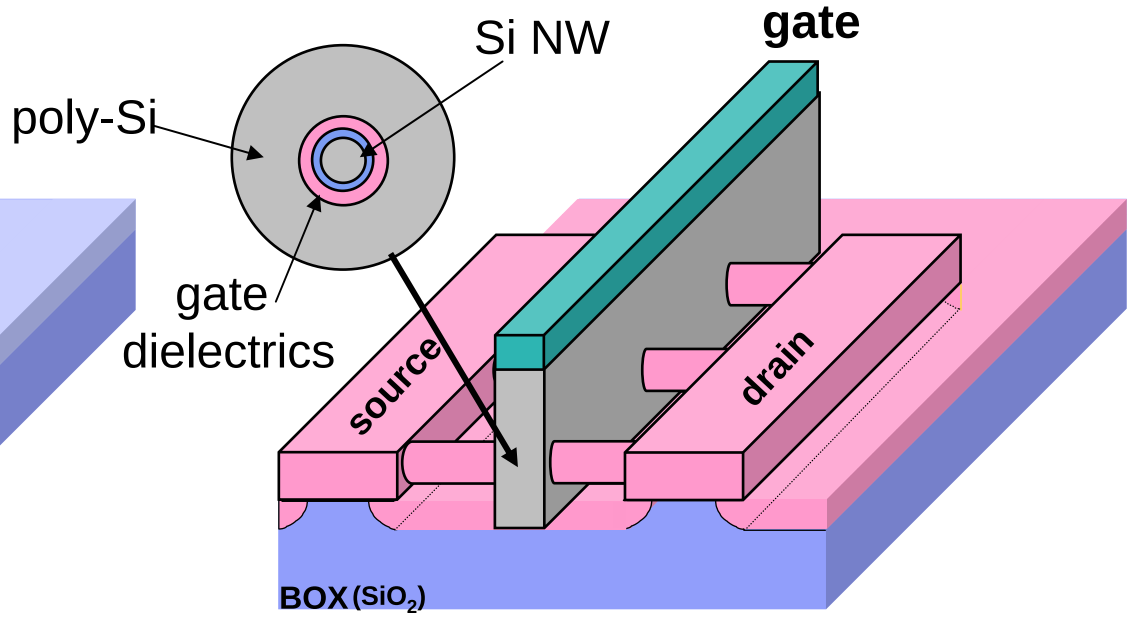
Si NW device



Si nanowire CMOS device fabrication

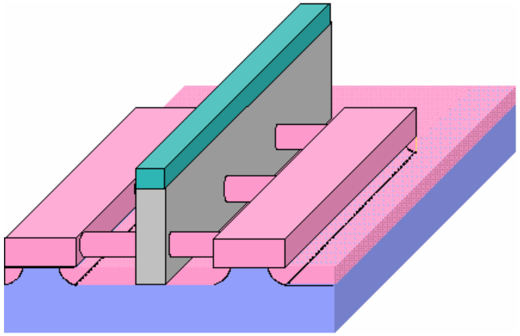
- **"top-down" Si nanowire CMOS device**
  - fabricated using Si on Insulator (SOI), electron beam lithography, and semiconductor processing methods (RIE, wet etching, thin film depositions PVD/CVD/ALD, etc.)
- **Int. Electron Devices Meeting (IEDM) 2009:**
  - **"High Performance and Highly Uniform Gate-All-Around Silicon Nanowire MOSFETs with Wire Size Dependent Scaling,"** S. Bangsaruntip, G.M. Cohen, A. Majumdar, Y. Zhang, S.U. Engelmann, N.C.M. Fuller, L.M. Gignac, S. Mittal, J.S. Newbury, M. Guillorn, T. Barwicz, L. Sekaric, M.M. Frank, and J.W. Sleight, IBM T. J. Watson Research Center



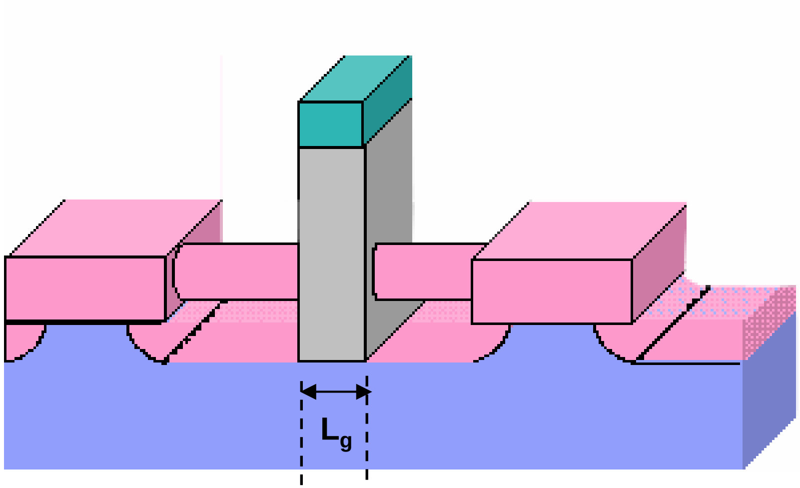


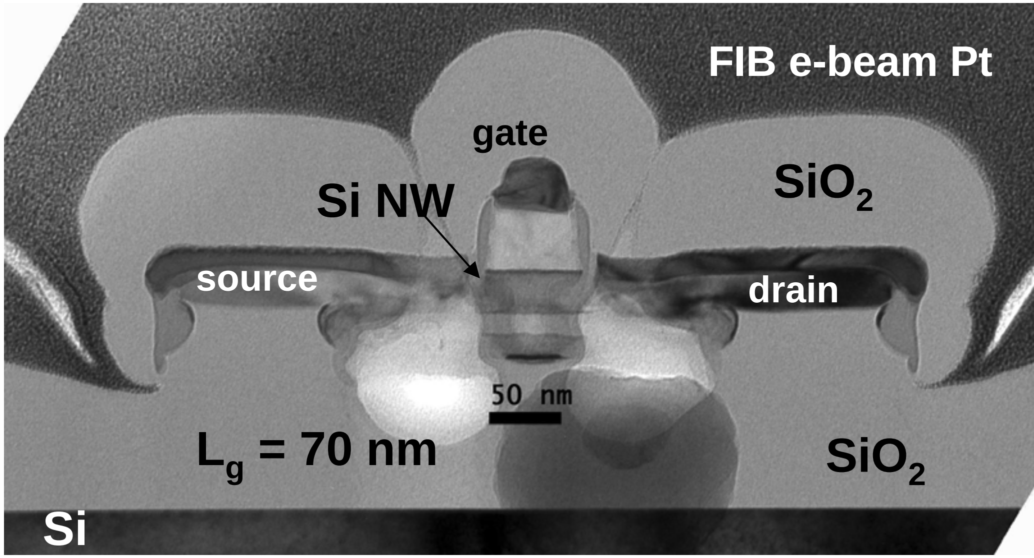
TEM sections required to understand electrical data

1. XTEM along NW:
   -measure gate length, L_g

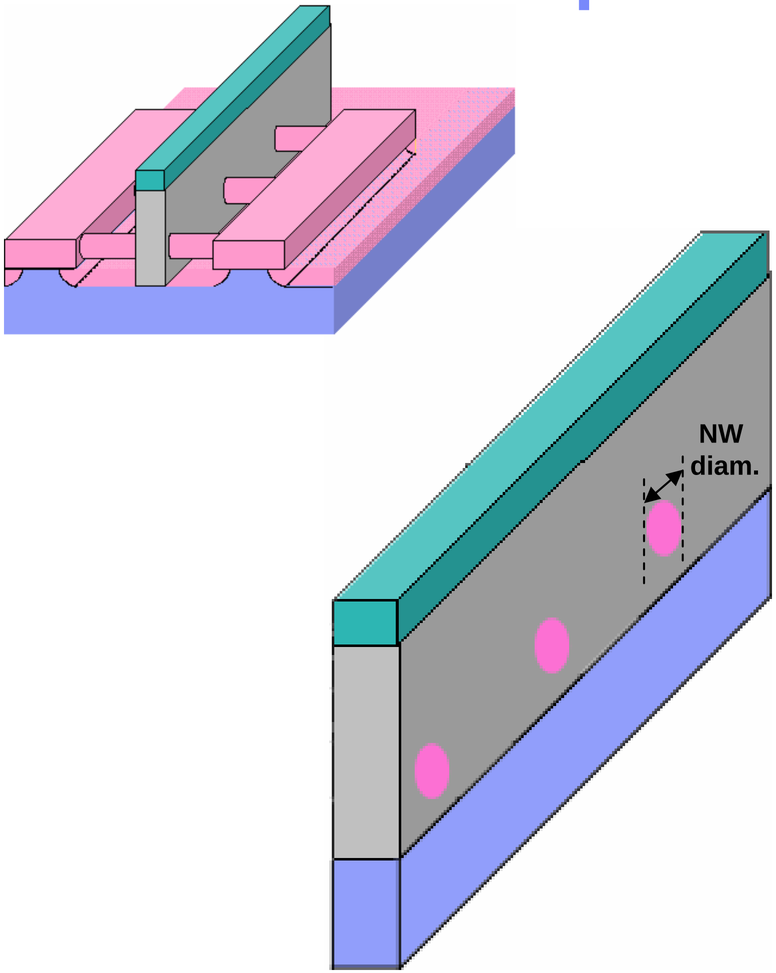


TEM image of NW sectioned along NW direction



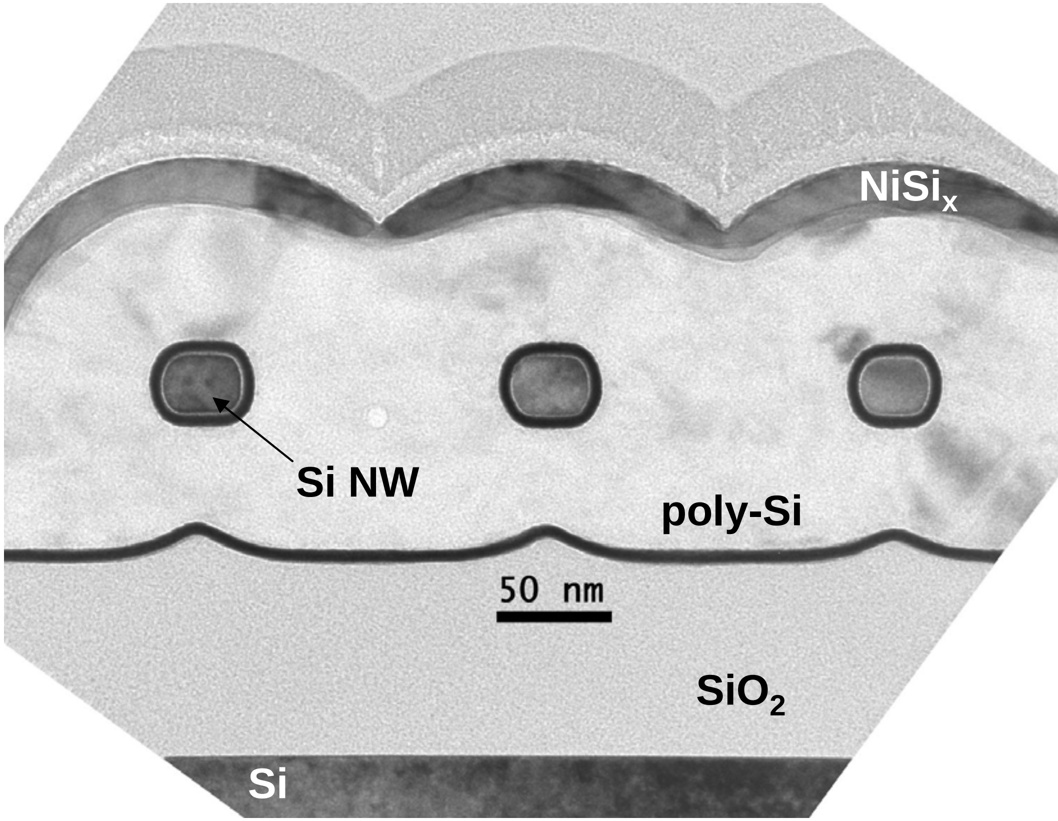


TEM sections required to understand electrical data



2. XTEM along NW:
-measure NW diameter and shape

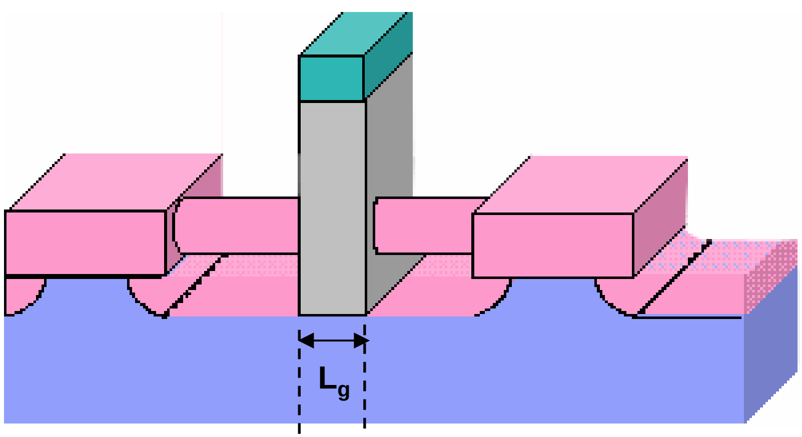
TEM image of NW sectioned perpendicular to NW

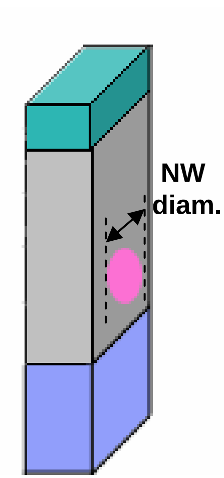


TEM sections required to understand electrical data

1. XTEM along NW:
-measure gate length, L_g

2. XTEM along NW:
-measure NW diameter and shape



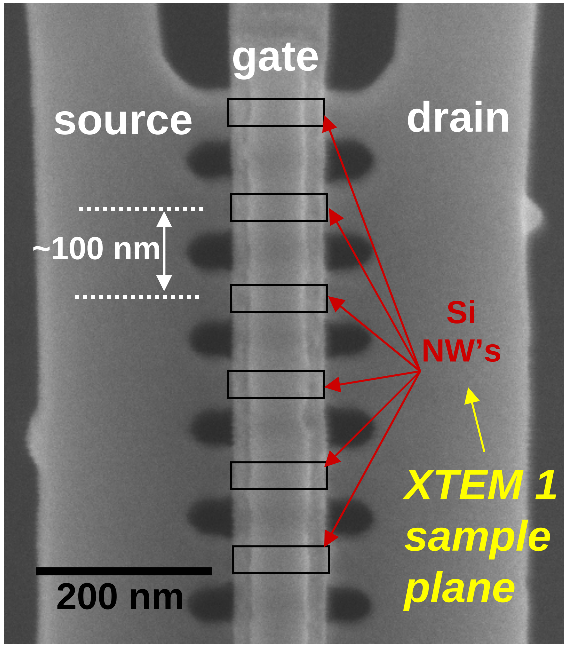


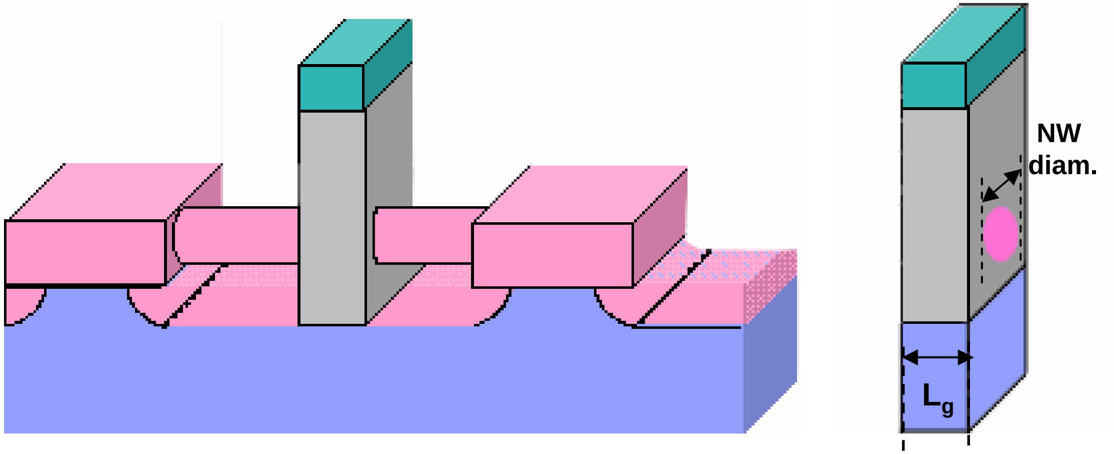
Either of these types of X-TEM sections are challenging individually:
- **NW diameters <30 nm, pitch ~100 nm, gate width < 100 nm**
- **requires state-of-the-art dualbeam FIB and highly skilled operator**

It is ideal to have both measurements from 1 XTEM sample

X-TEM prepared along NW

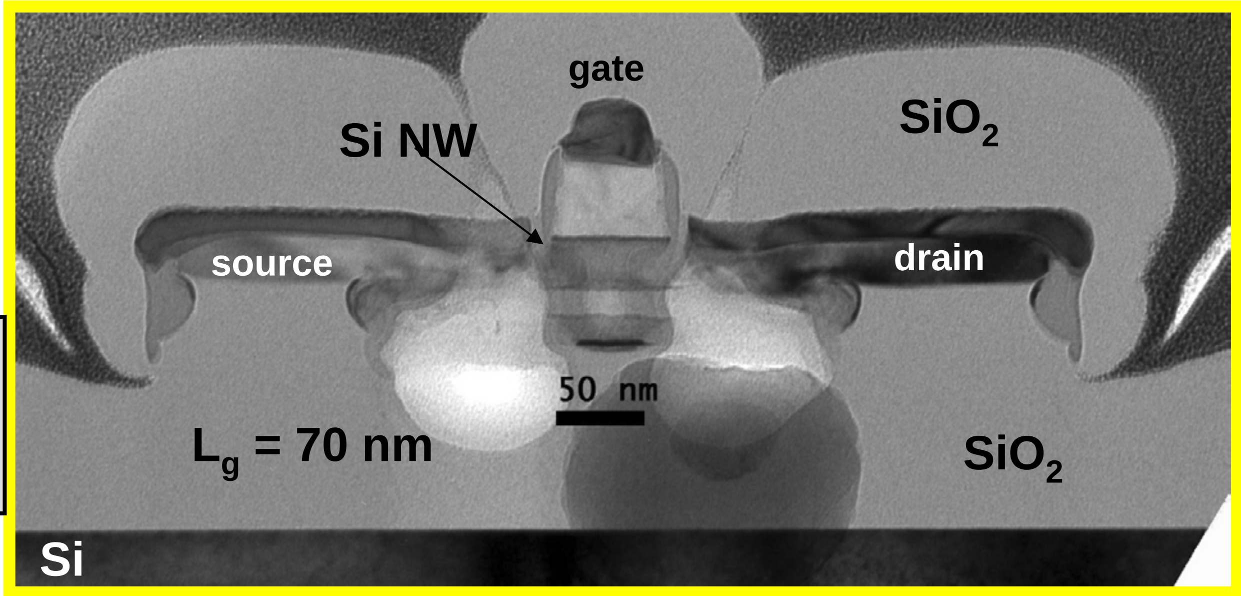
SEM image of NW device





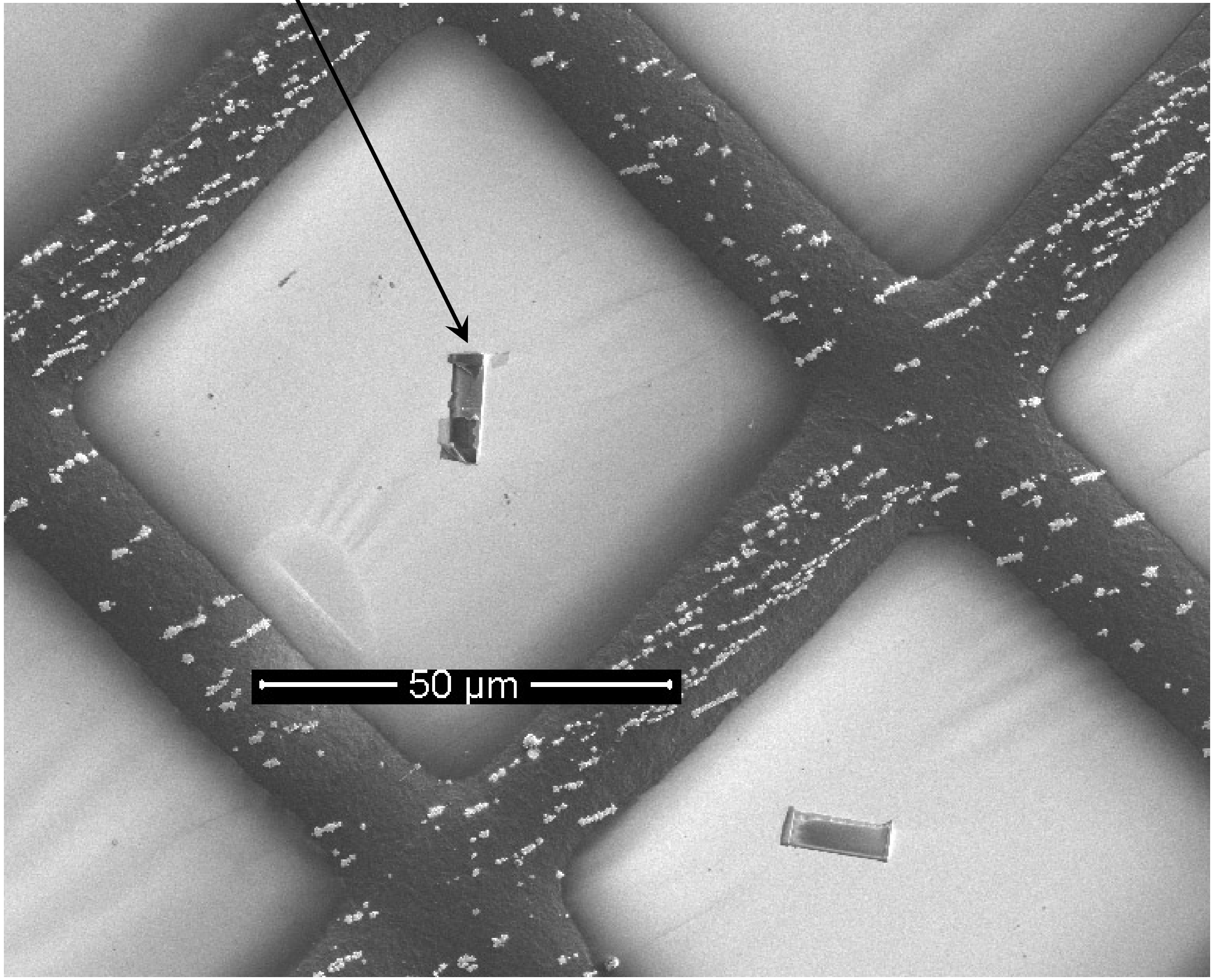
-from this XTEM 1 sample another XTEM 2 sample was prepared

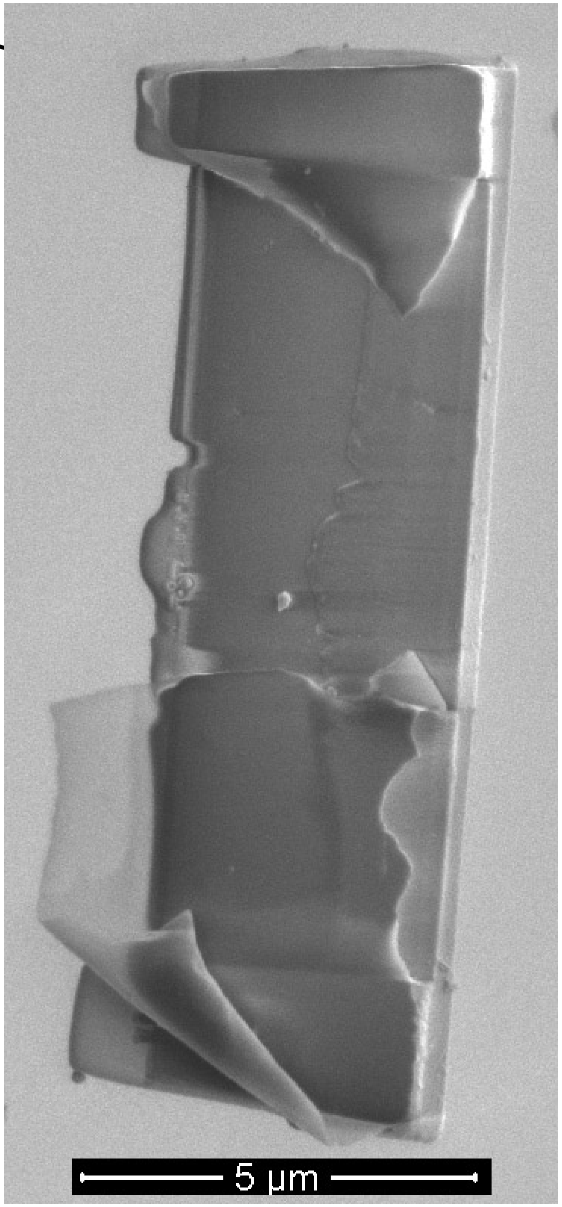
X-TEM image of NW device: sectioned along NW



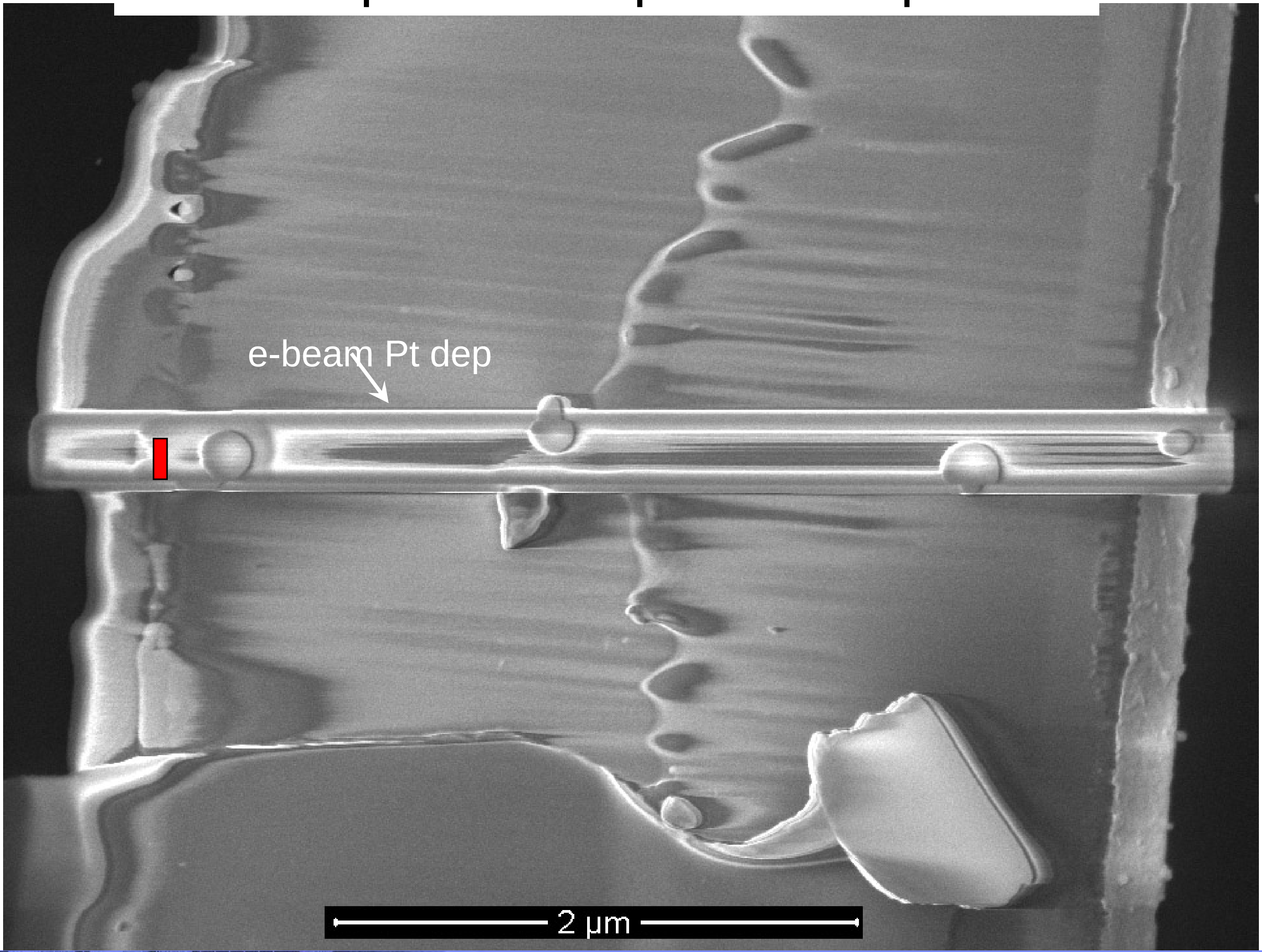
XTEM sample along NW on C membrane

- **sample mounted in FIB on "flip-stage": flat 90º**
- **orientation of sample very important for attachment of probe for in-situ lift-out**

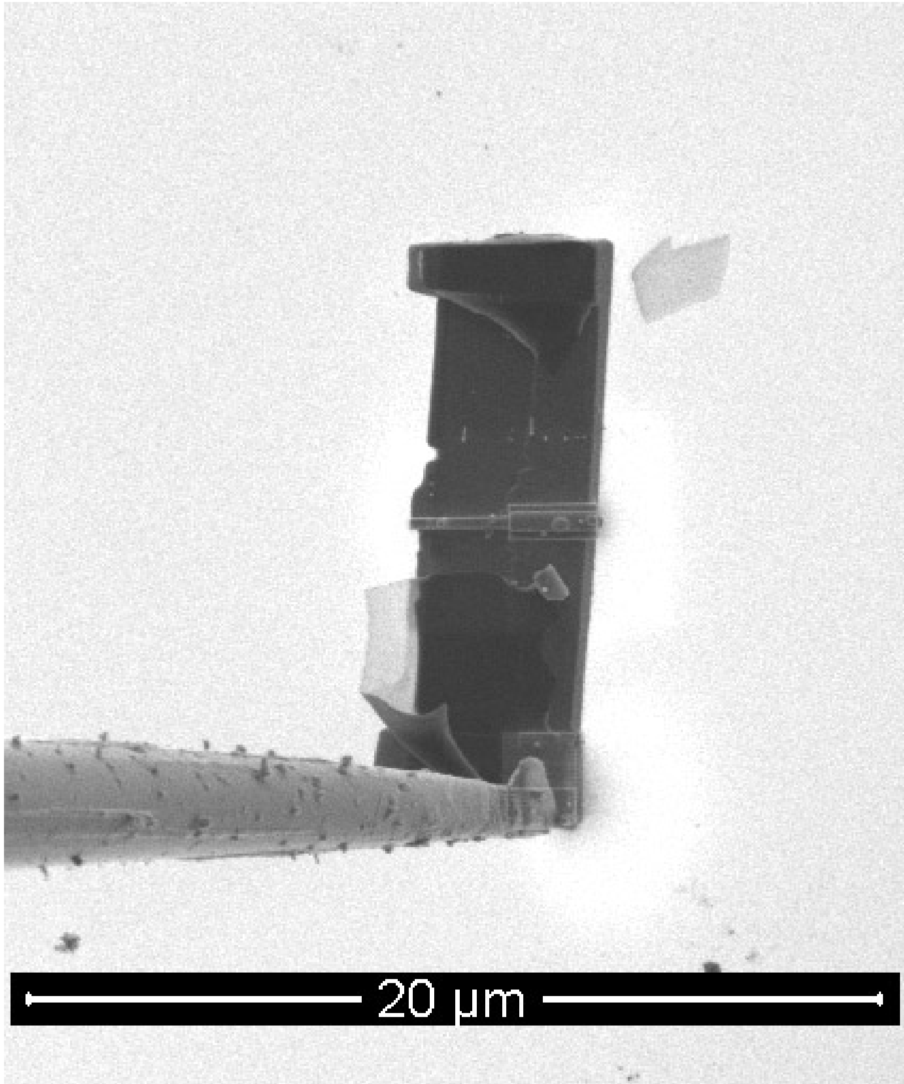




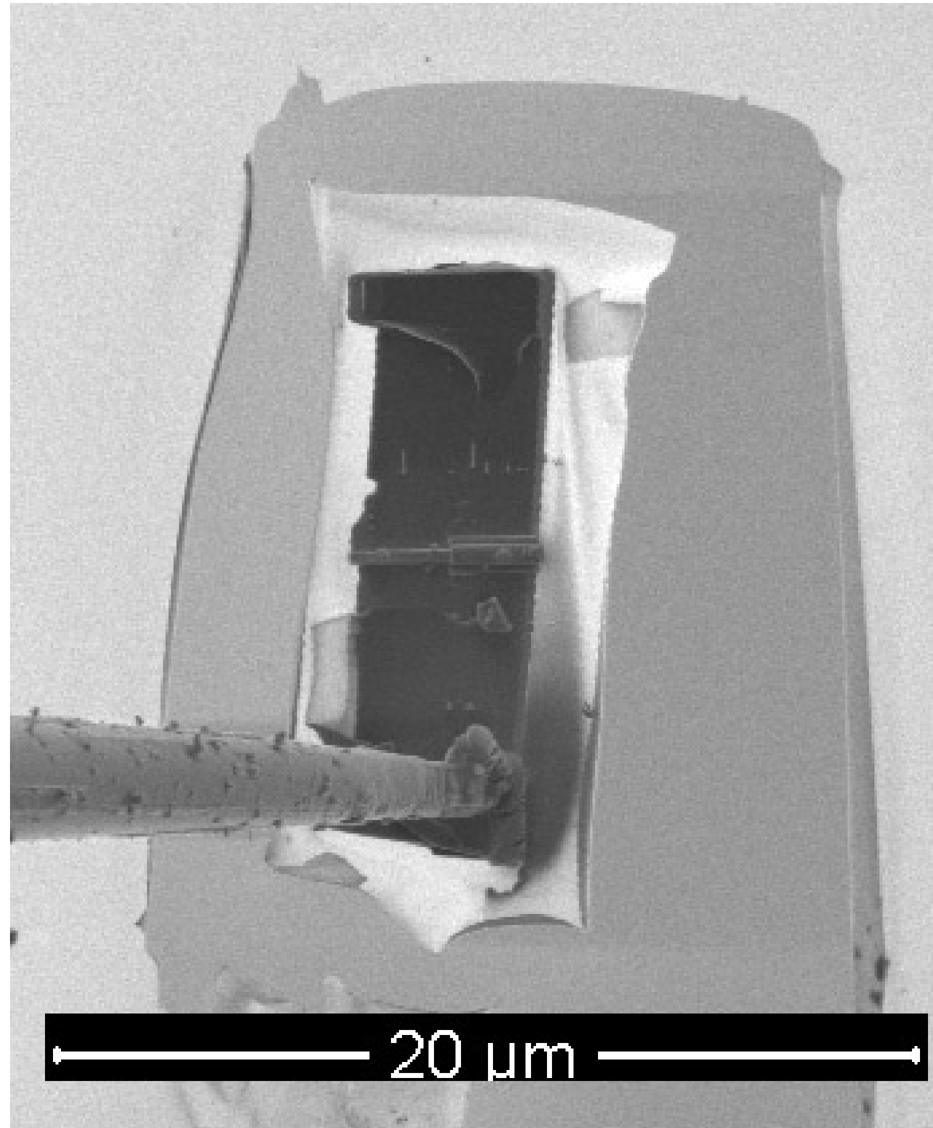
e-beam Pt deposited on sample surface for protection

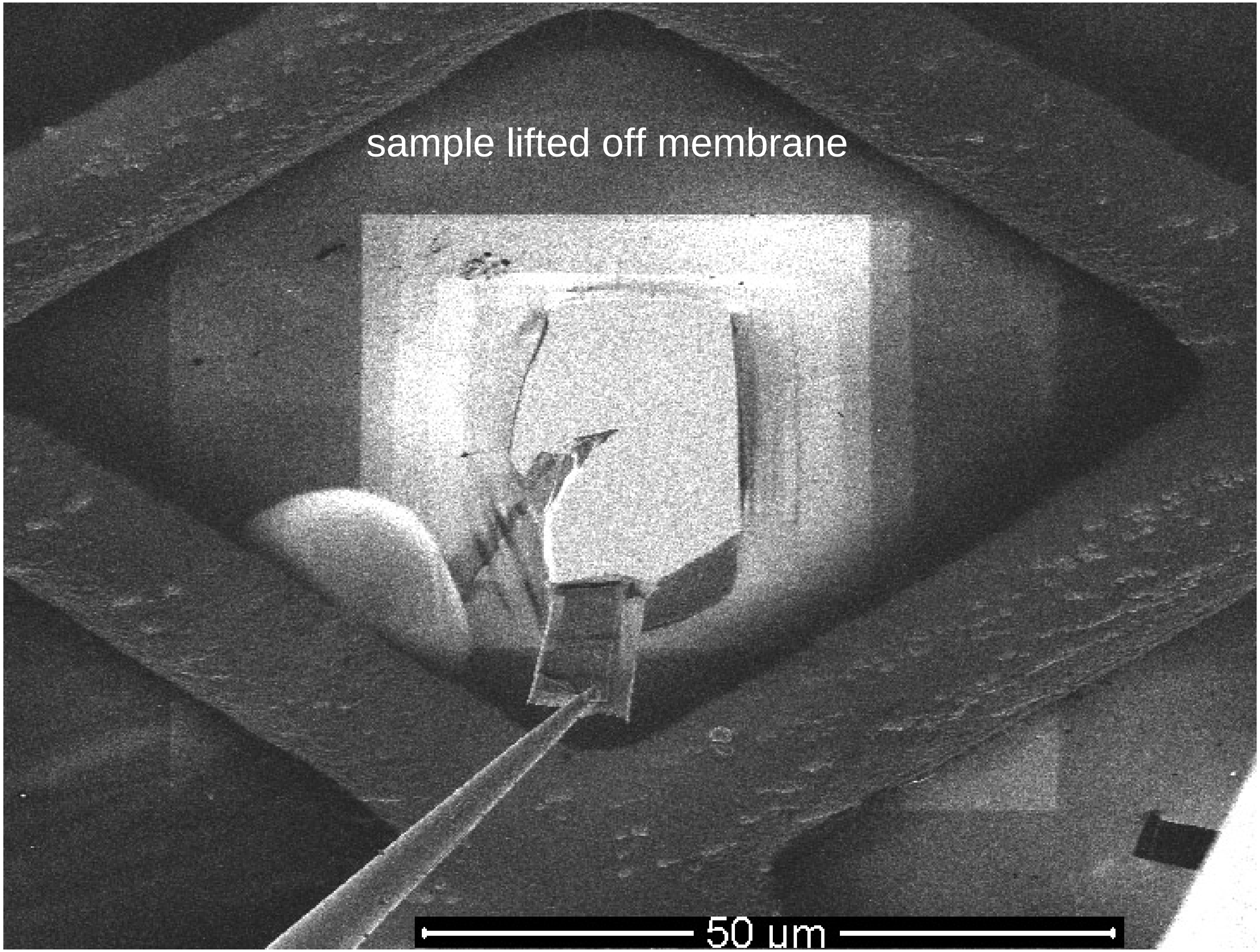


probe is attached to ex-situ lift-out sample

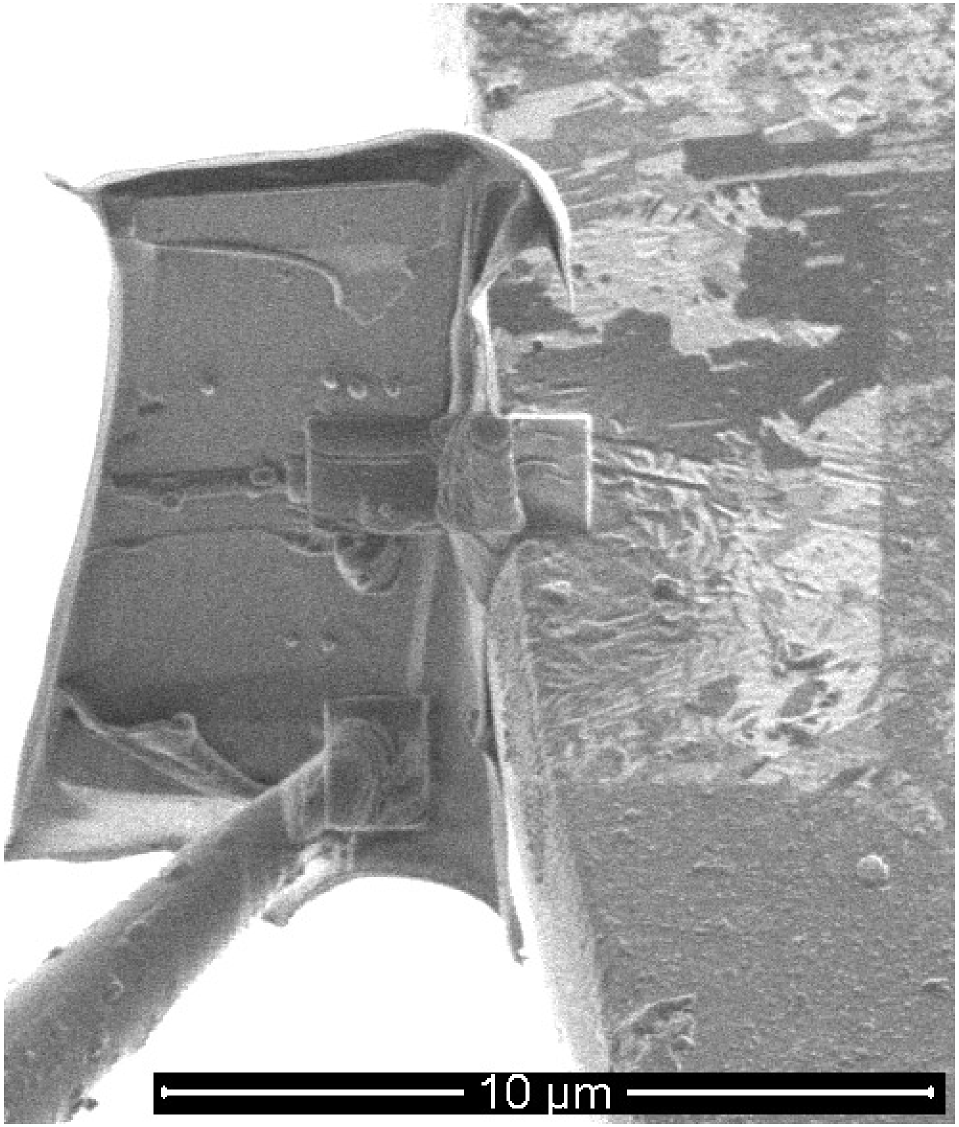


C membrane cut away with FIB

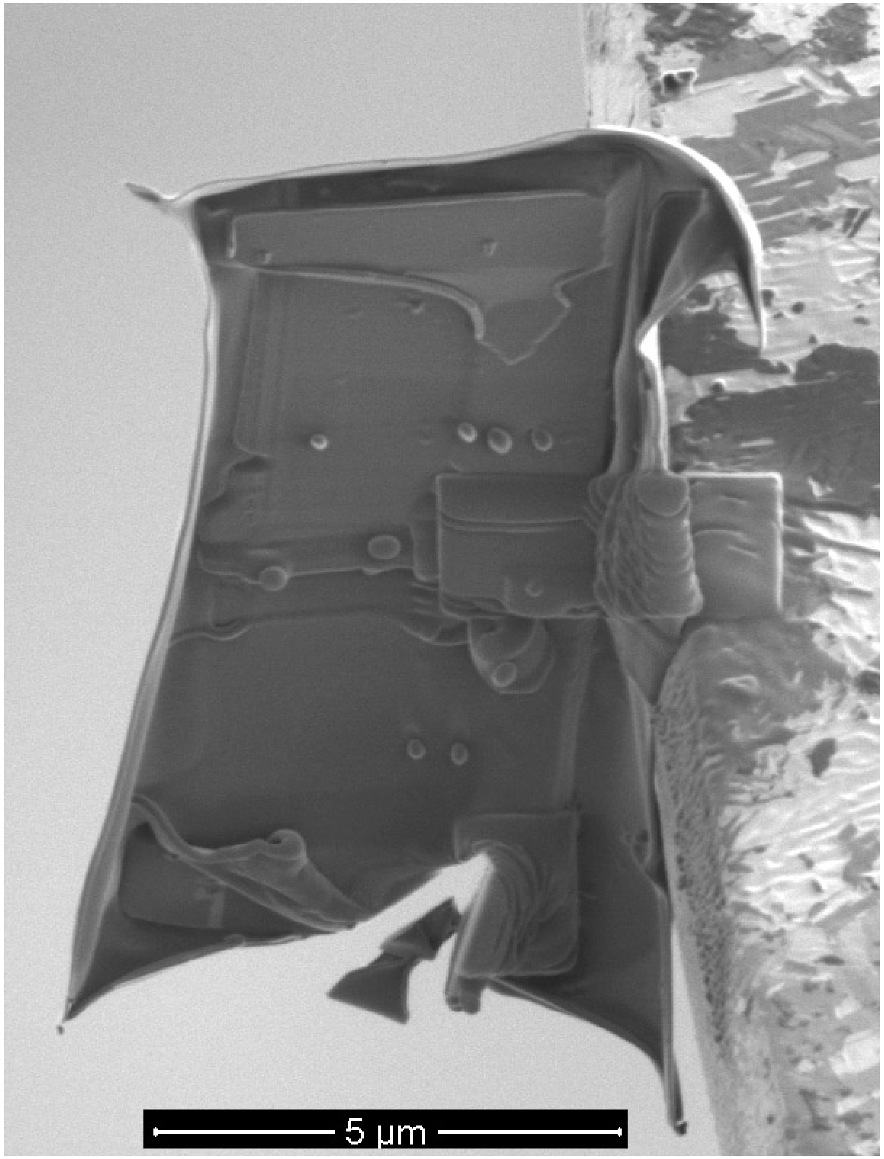



sample lifted off membrane
50 um

ion image: sample on finger

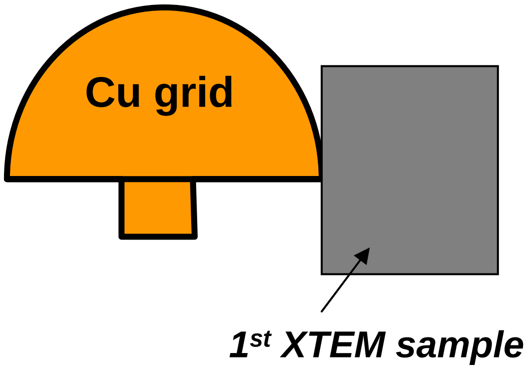


probe is released from sample

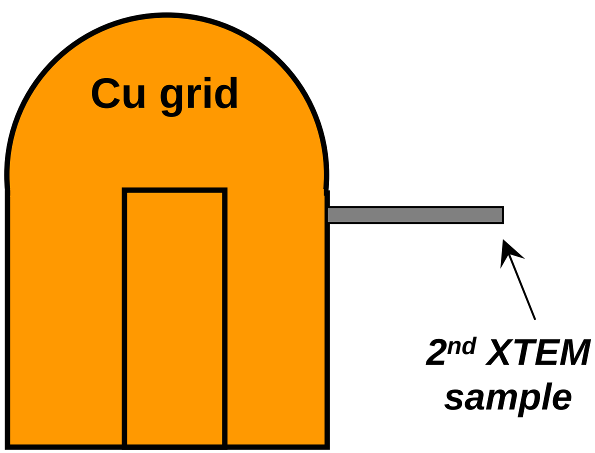


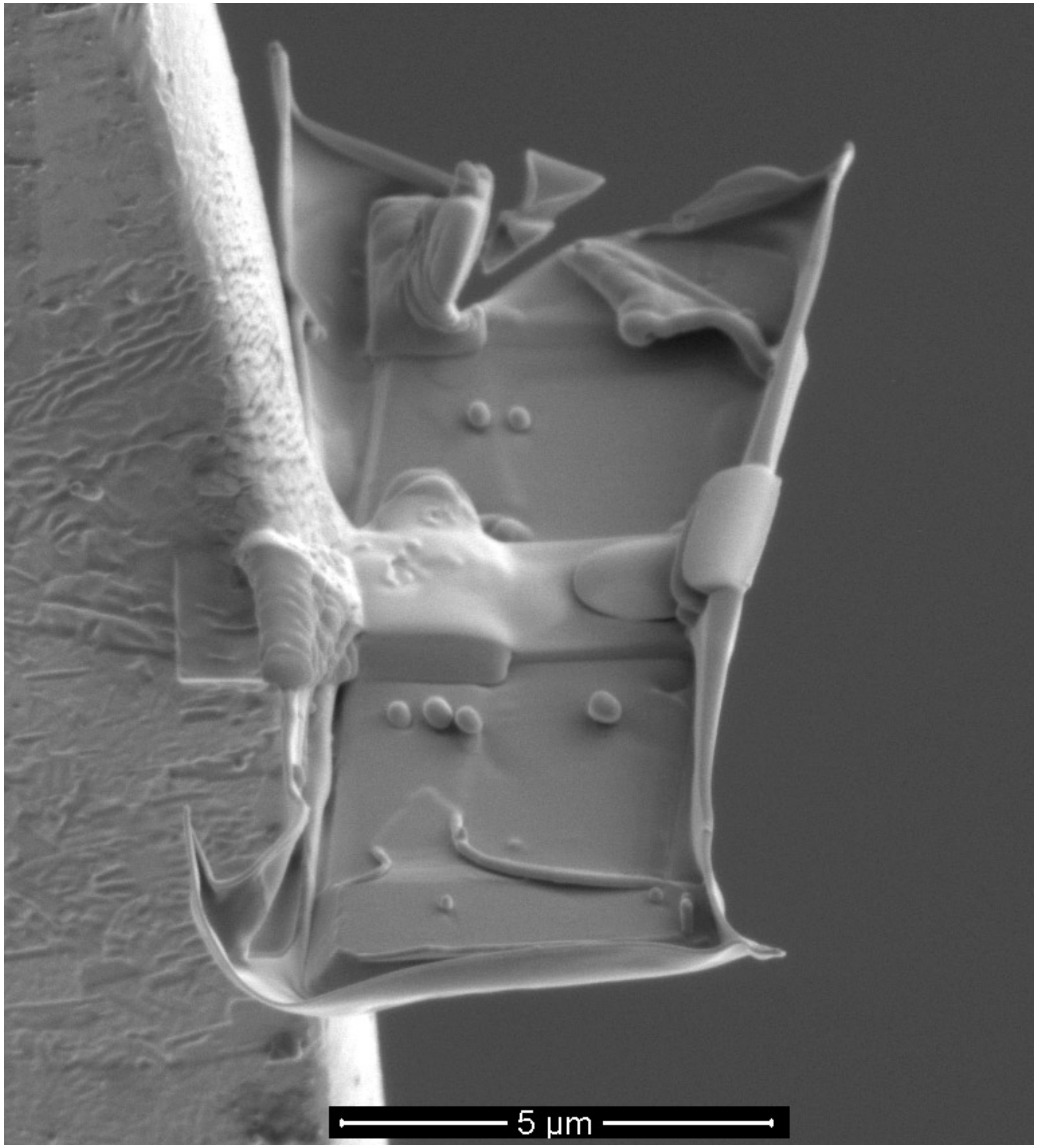
Sample is thinned in FIB

topdown diagram of sample on grid
(direction of Ga^+ beam to thin sample)



sideview diagram of sample on grid
(direction of TEM e^- beam viewing 2nd XTEM)





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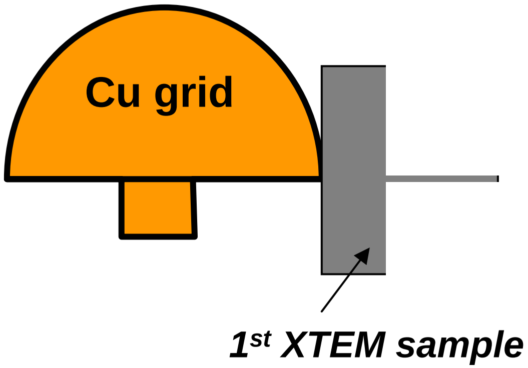

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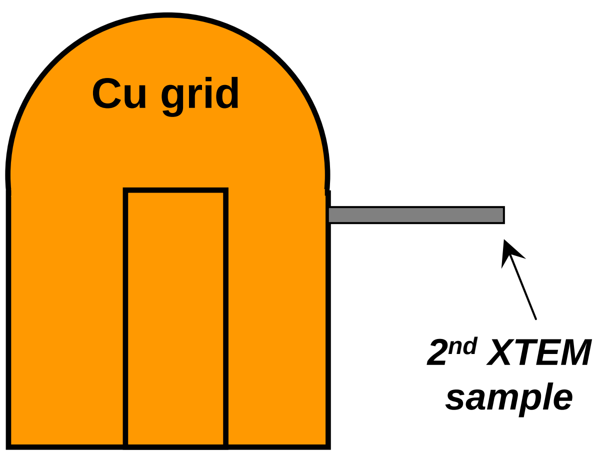
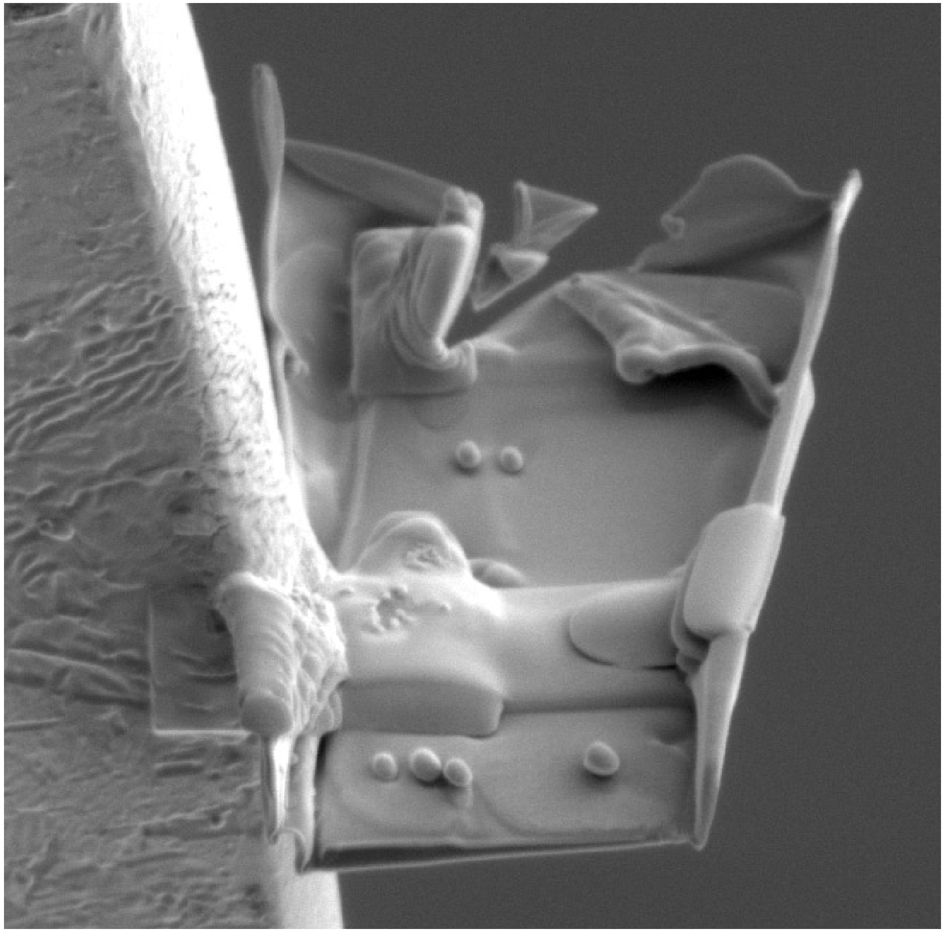
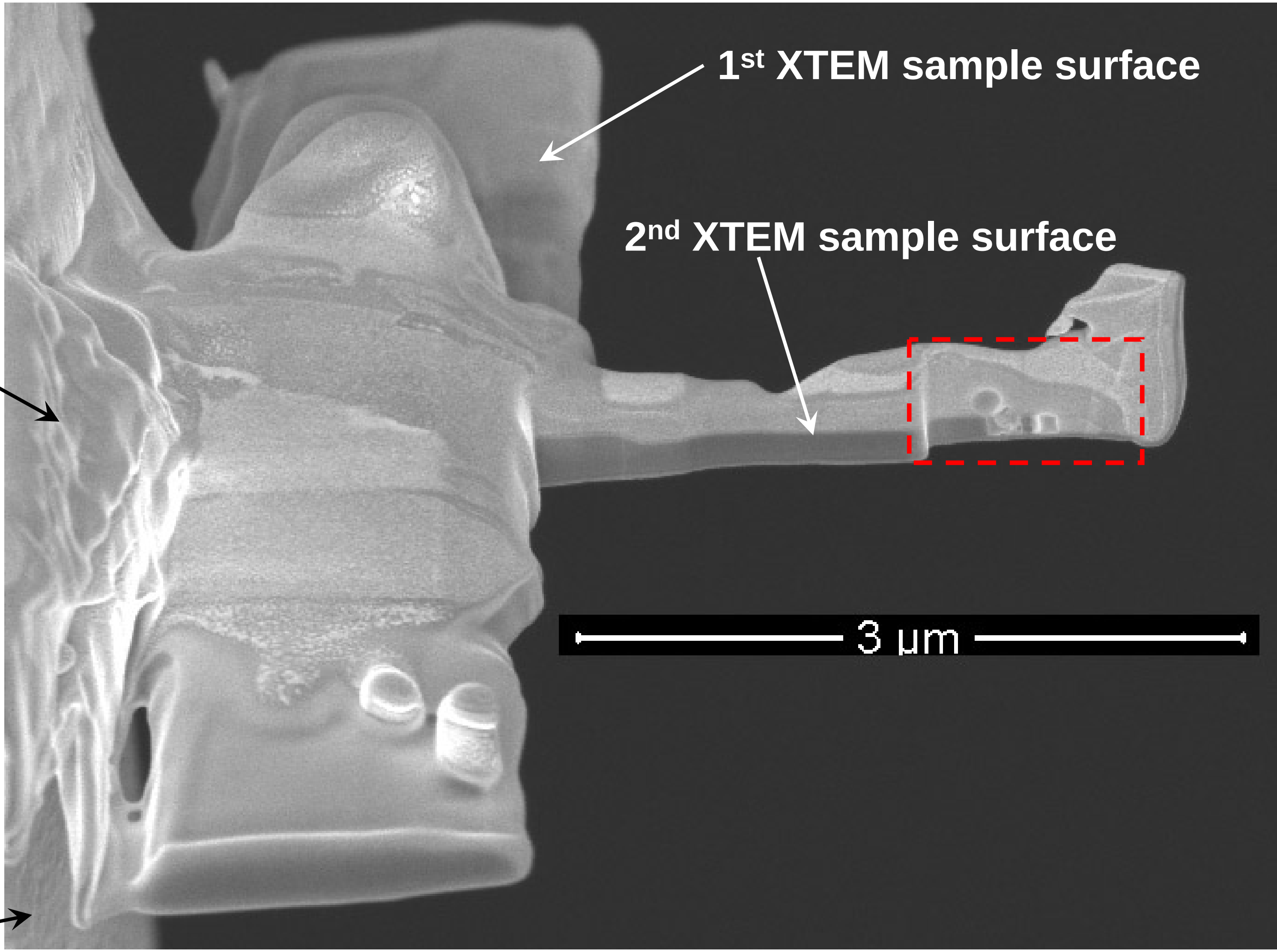




Final 2nd XTEM sample:

• **FIB thinning performed until NW seen on both sides of sample**

Pt used to attach 1st XTEM sample to Cu finger

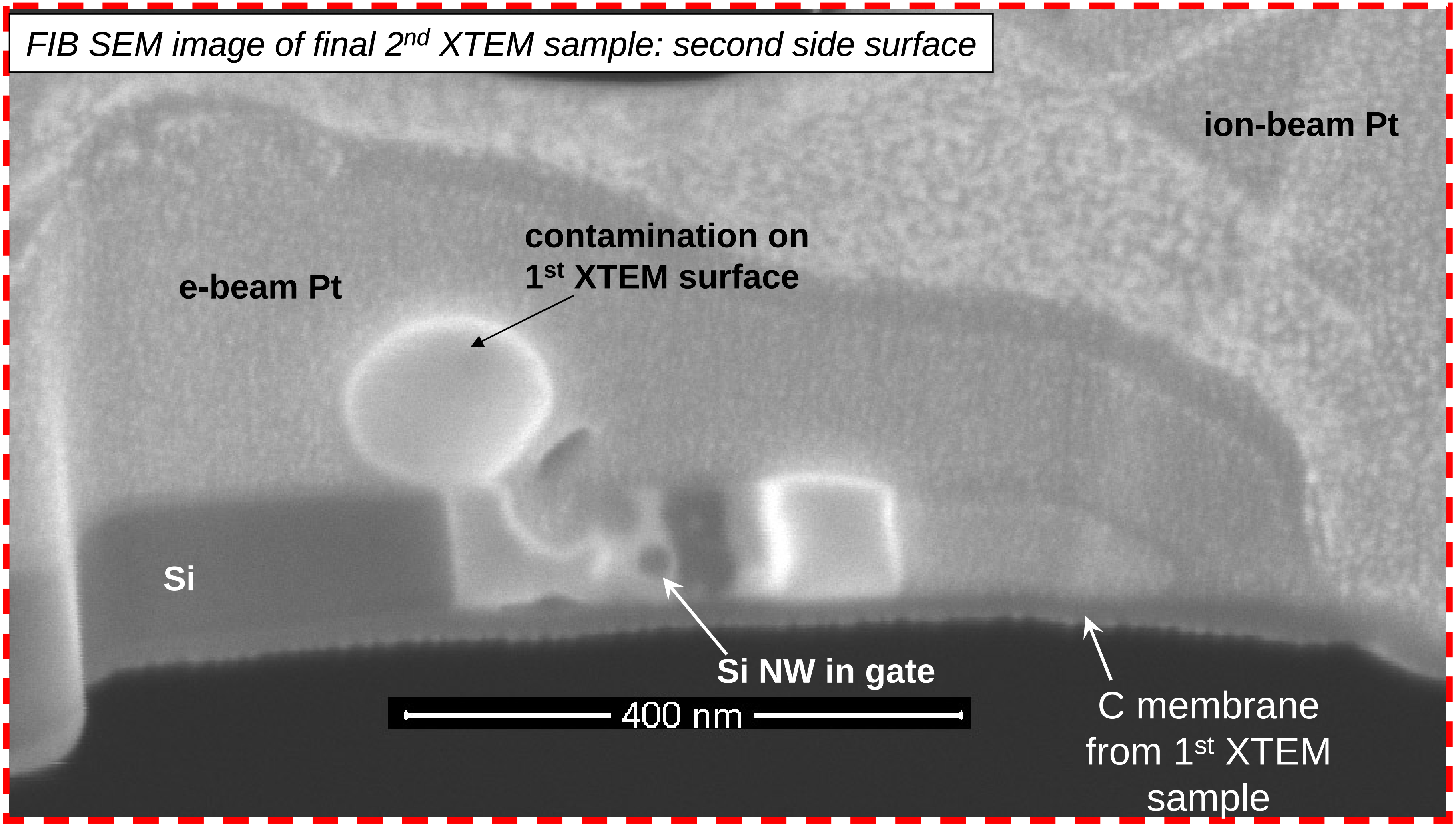


Cu grid finger

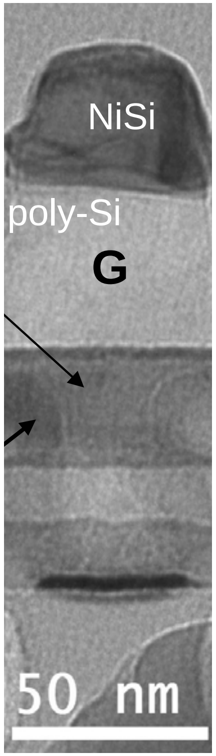
Final 2nd XTEM sample:

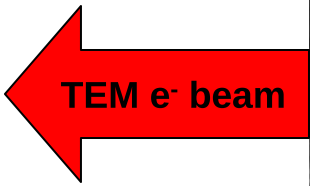
• FIB thinning performed until NW seen on both sides of sample

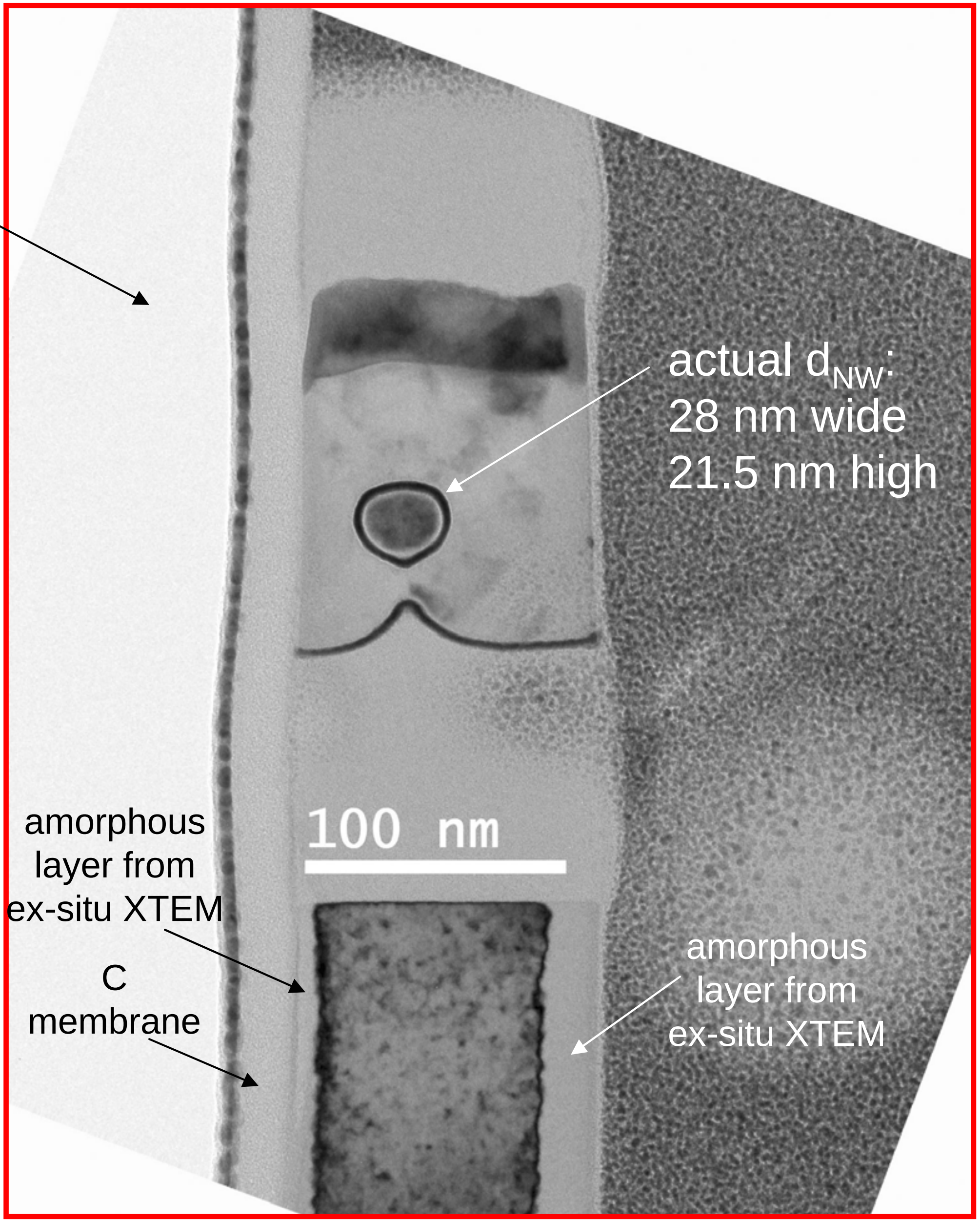
FIB SEM image of final 2nd XTEM sample: second side surface



Ex-situ lift out X-TEM sample along NW:
-sectioned again by in-situ lift out along the gate







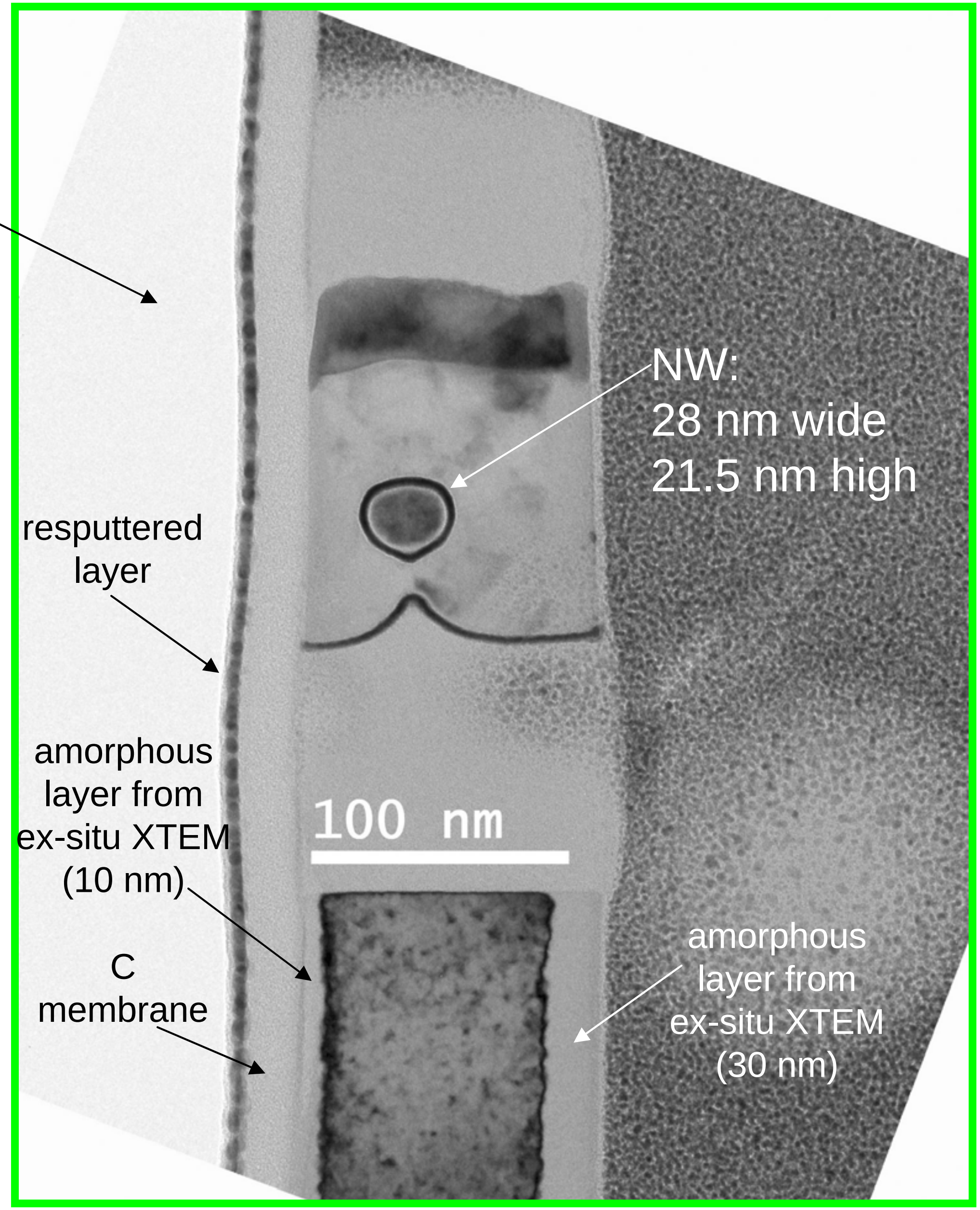
- L_g and NW_{diam} were measured in the same electrically tested device
- electrical data difficult to interpret without both of these measurements

Ex-situ lift out X-TEM sample along NW:
-sectioned again by in-situ lift out along the gate

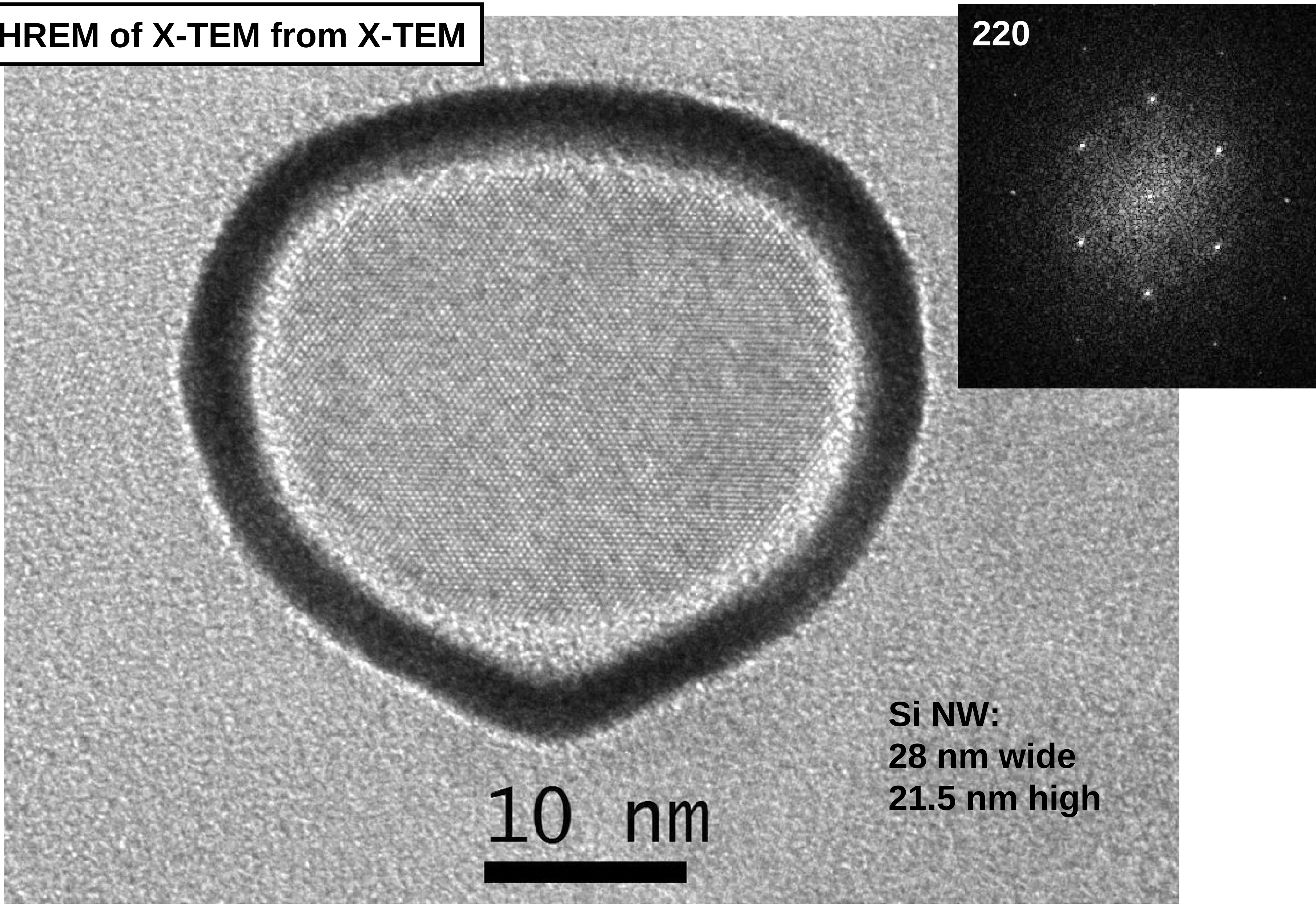
Amorphous layer thicker on right side of sample
- **more low keV clean on one side?**
- **e-beam Pt deposition causes damage?**

Si NW dimensions:
- **28 nm wide**
- **21.5 nm high**

Center NW in XTEM 1 section
- **do not damage or amorphize NW**



HREM of X-TEM from X-TEM



Conclusions:

- **an XTEM sample was successfully prepared from an XTEM on the first attempt**
- **this sample showed that the original ex-situ XTEM sample was 110 nm thick**
- **the C membrane and amorphous damage regions in single crystal Si were seen in this section from the ex-situ sample preparation**
  - the amorphous damage was 10 nm on one side and 30 nm on the other side of the sample
  - the difference could be due to:
    - more low energy cleaning on one side versus the other
    - e-beam Pt deposition might have damaged the Si surface
- **physical measurements:**
  - gate length is 70 nm
  - Si NW dimensions: 28 nm wide, 21.5 nm high
- **broke the barrier where one or the other physical measurement could be obtained from a specific electrically tested Si NW device**

Next:

- **Multiple XTEM's from 1 XTEM of sub-10 nm diameter NW devices**
  - abstract submitted to Microscopy & Microanalysis 2010